

**Application No.: 10/814,306**

**AMENDMENT TO CLAIMS**

1. (Currently amended) A simulator apparatus comprising:  
~~a plurality of simulator models each including a functional model for a CPU constituting a system to be simulated;~~  
~~a simulator model including a functional model for hardware to be connected to buses linked to the corresponding CPU;~~  
a plurality of simulator models each including a functional model workable as a CPU constituting a system to be simulated, peripheral hardware or buses connecting the peripheral hardware to the CPU;  
plural types of interfaces included in each of the simulator models and enabling plural types of simulators for various uses to access to the functional models; and  
a simulator controlling device for selecting any of the plural types of the interfaces and accessing the respective functional models via the selected interfaces.
2. (Original) A simulator apparatus as claimed in Claim 1, wherein  
the interfaces for the respective functional models comprise an interface usable in a simulator for verifying software.
3. (Original) A simulator apparatus as claimed in Claim 1, wherein  
the interfaces for the respective functional models comprise an interface usable in a simulator for verifying hardware.

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4. (Original) A simulator apparatus as claimed in Claim 1, wherein  
the interfaces for the respective functional models comprise an interface usable in a  
simulator for verifying a system.
5. (Original) A simulator apparatus as claimed in Claim 1, wherein  
the interfaces for the respective functional models comprise an interface usable in  
debugging.
6. (Previously presented) A simulator apparatus as claimed in Claim 1, wherein  
an interface to perform precise simulation for the system at clock level is comprised.
7. (Cancelled)
8. (Original) A simulator apparatus as claimed in Claim 1, wherein  
the interfaces for the respective functional models comprise an interface for extension  
usable in performance analysis.